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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 09/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,138	DUCKMAN, DAVID JAMES	
	Examiner	Art Unit	
	Hong C. Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-24 are presented for examination. This office action is in response to the application filed on 9/22/2003.

Information Disclosure Statement

2. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

Drawings

3. The drawings are objected to because:

Figures 1 and 2 are is described as prior art on pages 1-3, but is not labeled as such. In Figure 3, references for 302 and 304 are missing (see page 8 lines 23+). Correction is required.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. "tightly coupled processor", "generalized queue", "put and get pointers", and "specialized register" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Claim Objections

5. Claims 9-11 are objected to because of the following informalities: Claims 9-11 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. It appears that claims 9-11 are introduced new limitations rather further limiting previous claims. Also claims 10-11 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Liu et al. (Liu) U.S. Patent Application Pub. No. 2003/0126320.

As to claim 1, AAPA discloses an apparatus for coordinating communications between a plurality of tightly coupled processors (page 2 lines 1-2), comprising: one or

more generalized queues (page 2 line 24, QDR RAM) communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors.

However, AAPA does not specifically disclose each queue having a start location, an end location, a put pointer for indicating a next location in the queue into which an entry is to be supplied, and a get pointer for indicating a next location in the queue from which a entry is be received; and one or more specialized registers communicatively couplable to the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment; wherein the generalized queues and specialized registers are configurable in accordance with programs executable in the tightly coupled processors.

Liu discloses each queue having a start location (Fig. 3, Entry 0), an end location (Fig. 3 Entry n), a put pointer (Fig. 3 putptr) for indicating a next location in the queue into which an entry is to be supplied, and a get pointer (Fig. 3 ref. getptr) for indicating a next location in the queue from which a entry is be received; and one or more specialized registers (Fig. 3 Ref. 310) communicatively couplable to the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment; wherein the generalized queues and specialized registers are configurable (block 83 line 2 and line 9-11) in accordance with

programs executable in the tightly coupled processors for the purpose of improving I/O processing speed (block 3).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate each queue having a start location, an end location, a put pointer for indicating a next location in the queue into which an entry is to be supplied, and a get pointer for indicating a next location in the queue from which a entry is be received; and one or more specialized registers communicatively couplable to the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment; wherein the generalized queues and specialized registers are configurable in accordance with programs executable in the tightly coupled processors as taught by Liu into the system of AAPA for the advantages stated above.

As to claim 2, AAPA and Liu disclose the invention as claimed. Liu further discloses at least one specialized register for storing the put pointer and the get pointer of a generalized queue associated with the specialized register to assist in supplying entries into the generalized queue, receiving entries from the generalized queue, and determining whether the generalized queue is empty, full, not full, or not empty (blocks 75-76).

As to claim 3, AAPA and Liu disclose the invention as claimed. Liu further discloses at least one specialized register for storing an end location of a generalized queue associated with that specialized register to dynamically adapt a size of the generalized queue to the current operating environment (block 67).

As to claim 4, AAPA and Liu disclose the invention as claimed. Liu further discloses comprising at least one specialized register for storing requests from two or more processors to reset a generalized queue being utilized to pass entries between the processors, in order to facilitate a coordinated reset of that generalized queue (blocks 73 and 91).

As to claim 5, AAPA and Liu disclose the invention as claimed. Liu further discloses at least one specialized register for storing attention conditions from one processor destined for another processor (block 73, READY signal).

As to claim 6, AAPA and Liu disclose the invention as claimed. Liu further discloses at least one specialized register for storing whether the generalized queues are not empty or not full (blocks 75-76).

As to claim 7, AAPA and Liu disclose the invention as claimed. Liu further discloses at least one specialized register for storing an enable indicating whether an

attention condition destined for one processor will be visible to that processor (block 73).

As to claim 8, AAPA and Liu disclose the invention as claimed. Liu further discloses at least one specialized register for storing an enable indicating whether an indicator of whether the generalized queue is not empty or not full destined for one processor will be visible to that processor (block 73).

As to claim 9, AAPA and Liu disclose the invention as claimed. AAPA further discloses the one or more tightly coupled processors for providing I/O processing and physical connectivity between a host device coupled to a host bus and external data storage devices coupled to one or more storage area networks (page 2 lines 1-12).

As to claim 10, AAPA and Liu disclose the invention as claimed. AAPA further discloses a host bus adapter (HBA) (page 2 lines 1-3) comprising the interface controller chip of claim 9, wherein the host bus is a PCI or PCI-X bus (page 2 line 21) and the external data storage devices communicate over the one or more storage area networks using fibre channel (FC) protocols (page 2 line 17).

As to claim 11, AAPA and Liu disclose the invention as claimed. Liu further discloses a server computer comprising the HBA (page 2 lines 1-12).

As to claim 12, AAPA discloses in a multi-processor system including a plurality of tightly coupled processors (page 2 lines 1-2) and one or more generalized queues (page 2 line 24, QDR RAM) communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors.

However, AAPA does not specifically disclose an apparatus for coordinating communications between the tightly coupled processors, comprising: one or more specialized registers communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable in the tightly coupled processors for adjusting a size and location of the generalized queues to dynamically adapt the generalized queue to the current operating environment; informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full; and enabling attention conditions to be passed between the tightly coupled processors.

Liu discloses an apparatus for coordinating communications between the tightly coupled processors, comprises one or more specialized registers (Fig. 3 Ref. 310) communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable (block 83 line 2 and line 9-11) in the tightly coupled processors for adjusting a size and location of the generalized queues to dynamically (block 67) adapt the generalized queue to the current operating environment; informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full (blocks 75-76); and enabling attention conditions to be passed between the tightly coupled processors (block 73) for the purpose of improving I/O processing speed (block 3).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate an apparatus for coordinating communications between the tightly coupled processors, comprising: one or more specialized registers communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable in the tightly coupled processors for adjusting a size and location of the generalized queues to dynamically adapt the generalized queue to the current operating environment; informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full; and enabling attention conditions to be passed between the tightly coupled processors as taught by Liu into the system of AAPA for the advantages stated above.

As to claim 13, AAPA discloses an apparatus for providing I/O processing and physical connectivity between a host device coupled to a host bus and external data storage devices (page 1 lines 10- 13) coupled to one or more storage area networks (page 1 line 16), comprises a plurality of tightly coupled processors (page 2 lines 1-3) for coordinating a transfer of information between the host device and the external storage devices; one or more generalized queues (page 2 line 24, QDR RAM) communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors

However, AAPA does not specifically disclose one or more specialized registers communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable in the tightly coupled processors for assisting

the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment.

Liu discloses one or more specialized registers (Fig. 3 Ref. 310) communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable (block 83 line 2 and line 9-11) in the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment (block 83 line 2 and line 9-11) for the purpose of improving I/O processing speed (block 3).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate one or more specialized registers communicatively couplable to the tightly coupled processors and configurable in accordance with programs executable in the tightly coupled processors for assisting the tightly coupled processors in utilizing the generalized queues for interprocessor communications and adapting the generalized queues to match a current operating environment as taught by Liu into the system of AAPA for the advantages stated above.

As to claim 14, AAPA and Liu disclose the invention as claimed. Liu further discloses the tightly coupled processors are programmed for utilizing the one or more specialized registers to adjust a size and location of the generalized queues to

dynamically adapt the generalized queue to the current operating environment 9block 67); inform the tightly coupled processors when the generalized queues are empty, full, not empty, or not full; and enable attention conditions to be passed between the tightly coupled processors (blocks 75-76).

As to claim 15, AAPA discloses a method for coordinating communications between a plurality of tightly coupled processors (page 2 lines 1-2), comprises utilizing one or more generalized queues (page 2 line 24, QDR RAM) for storing and passing entries between the tightly coupled processors and facilitating interprocessor communications.

However, AAPA does not specifically disclose configuring one or more specialized registers to assist the tightly coupled processors in adapting and utilizing one or more generalized queues for storing; storing and retrieving information in the configured specialized registers for use in adapting the generalized queues to match a current operating environment; storing and retrieving information in the configured specialized registers for use in determining when entries may be supplied into or received from the generalized queues; and storing and retrieving attention conditions in the configured specialized registers to be passed between the tightly coupled processors.

Liu discloses configuring one or more specialized registers (Fig. 3 Ref. 310) to assist the tightly coupled processors in adapting and utilizing one or more generalized queues for storing; storing and retrieving information in the configured specialized

registers for use in adapting the generalized queues to match a current operating environment (block 83 line 2 and line 9-11); storing and retrieving information in the configured specialized registers for use in determining when entries may be supplied into or received from the generalized queues (block 83); and storing and retrieving attention conditions in the configured specialized registers to be passed between the tightly coupled processors (blocks 73 and 83) for the purpose of improving I/O processing speed (block 3).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate configuring one or more specialized registers to assist the tightly coupled processors in adapting and utilizing one or more generalized queues for storing; storing and retrieving information in the configured specialized registers for use in adapting the generalized queues to match a current operating environment; storing and retrieving information in the configured specialized registers for use in determining when entries may be supplied into or received from the generalized queues; and storing and retrieving attention conditions in the configured specialized registers to be passed between the tightly coupled processors as taught by Liu into the system of AAPA for the advantages stated above.

As to claim 16, AAPA and Liu disclose the invention as claimed. Liu further discloses for each generalized queue, the method further comprises storing, in the configured specialized registers, a put pointer (Fig. 3 Ref. putptr) for indicating a next location in the queue into which an entry is to be supplied and a get pointer (Fig. 3 Ref.

Ref. getptr) for indicating a next location in the queue from which a entry is be received, the get and put pointers for assisting in supplying entries into the generalized queue, receiving entries from the generalized queue (block 83), and determining whether the generalized queue is empty, full, not full, or not empty (blocks 75-76).

As to claim 17, AAPA and Liu disclose the invention as claimed. Liu further discloses for each generalized queue, the method further comprises storing, in the configured specialized registers, an end location of the generalized queue for dynamically adapting a size of the generalized queue to the current operating environment (blocks 67 and 83).

As to claim 18, AAPA and Liu disclose the invention as claimed. Liu further discloses for each generalized queue, the method further comprises storing, in the configured specialized registers, requests from two or more processors to reset the generalized queue in order to facilitate a coordinated reset of that generalized queue (blocks 73 and 91).

As to claim 19, AAPA and Liu disclose the invention as claimed. Liu further discloses changing the size of a generalized queue by performing a coordinated reset of the generalized queue and storing a new end location in the configured specialized registers (blocks 73 and 91).

As to claim 20, AAPA and Liu disclose the invention as claimed. Liu further discloses storing, in the configured specialized registers, attention conditions from one processor destined for another processor (block 73).

As to claim 21, AAPA and Liu disclose the invention as claimed. Liu further discloses storing, in the configured specialized registers, whether the generalized queues are not empty or not full (blocks 75-76).

As to claim 22, AAPA and Liu disclose the invention as claimed. Liu further discloses storing, in the configured specialized registers, an enable indicating whether an attention condition destined for one processor will be visible to that processor (block 73).

As to claim 23, AAPA and Liu disclose the invention as claimed. Liu further discloses storing, in the configured specialized register, an enable indicating whether an indicator of whether the generalized queue is not empty or not full destined for one processor will be visible to that processor (blocks 75-76).

As to claim 24, AAPA discloses in a multi-processor system including a plurality of tightly coupled processors (page 2 lines 1-2) and one or more generalized queues (page 2 line 24, QDR RAM) communicatively couplable to the tightly coupled processors for storing entries to be passed between the tightly coupled processors, a

method for coordinating communications between the tightly coupled processors, comprises utilizing the generalized queues for storing and passing entries between the tightly coupled processors and facilitating interprocessor communications

However, AAPA does not specifically disclose configuring one or more specialized registers to assist the tightly coupled processors in adapting; adjusting a size and location of the generalized queues in accordance with information stored in the specialized registers to dynamically adapt the generalized queues to the current operating environment; informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full in accordance with information stored in the specialized registers; and passing attention conditions between the tightly coupled processors in accordance with information stored in the specialized registers.

Liu discloses configuring one or more specialized registers (Fig. 3 Ref. 310) to assist the tightly coupled processors in adapting; adjusting a size and location of the generalized queues (blocks 67 and 83) in accordance with information stored in the specialized registers to dynamically adapt the generalized queues to the current operating environment; informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full (blocks 75-76) in accordance with information stored in the specialized registers; and passing attention conditions between the tightly coupled processors in accordance with information stored in the specialized registers (blocks 73 and 83) for the purpose of improving I/O processing speed (block 3).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate configuring one or more specialized registers to assist the tightly coupled processors in adapting; adjusting a size and location of the generalized queues in accordance with information stored in the specialized registers to dynamically adapt the generalized queues to the current operating environment; informing the tightly coupled processors when the generalized queues are empty, full, not empty, or not full in accordance with information stored in the specialized registers; and passing attention conditions between the tightly coupled processors in accordance with information stored in the specialized registers as taught by Liu into the system of AAPA for the advantages stated above.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
September 21, 2005